REMARKS

By this Amendment, claims 1-20 are amended. Thus, claims 1-20 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

In item 2 on page 2 of the Office Action, claims 1, 3 and 9-13 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yamaha (U.S. Patent Application Publication No. 2003/0003707). Further, in item 4 on page 3 of the Office Action, claims 2, 4-8 and 14-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaha in view of Nishitani et al. (U.S. 5,498,768).

Without intending to acquiesce to these rejections, independent claims 1, 6 and 8 have each been amended in order to more clearly illustrate the marked differences between the present invention and the applied references.

Accordingly, the Applicants respectfully submit that the present invention is clearly patentable over the applied references for the following reasons.

In conventional methods of manufacturing semiconductor elements, as described in the Background of the Invention section of the specification and in Figures 6-7, when a via-hole 5 is formed, an undesirable material (TiOx) 9 remains at the bottom of the via-hole 5. As a result, the TiOx 9 is left between the W plug 7 and the adhesive layer 6 of the first wiring layer 3. Since the TiOx remains in the via-hole (or between the adhesive layer 6 and the W plug 7), the resulting semiconductor element (or the via-hole 5) has a high resistance.

The present invention solves this problem by feeding only a single fluorine compound gas having a reduction function into the via-hole 15 prior to forming the W nucleus in the via-hole 15. In other words, only one reduction gas (WF_6, NF_3 or SiF_4) is

fed into the via-hole prior to the formation of the W nucleus in the via-hole 15 so that the undesired substance 9 is removed prior to the W nucleus being formed in the via-hole 15.

WF_6 is used as the single fluorine compound in the first embodiment of the present invention (step S11 in Figure 2). NF_3 is used as the single fluorine compound in the second embodiment of the present invention (step S21 in Figure 3). SiF_4 is used as the single fluorine compound in the third embodiment of the present invention (step S31 in Figure 4). Throughout the embodiments of the present invention, these fluorine compounds are used exclusively as the single fluorine compound gas having at least a reducing function which is fed into the via-hole prior to the formation of the W nucleus in the via-hole.

As a result, the present invention advantageously prevents the TiOx from being left between the W plug 7 and the adhesive layer of the first (lower) wiring layer 13. Accordingly, the present invention provides a method for manufacturing a semiconductor element having a low resistance and high reliability.

Claims 1, 6 and 8 each recite a method of manufacturing a semiconductor element having at least a substrate, a lower wiring layer, an upper wiring layer, a via-hole connecting the lower wiring layer to the upper wiring layer, and a W material filled in the via-hole. The method of claim 1 comprises feeding a single fluorine compound gas having a reducing function into the via-hole. The methods of claims 6 and 8 each comprises feeding a single fluorine compound gas into the via-hole to clean the via-hole and to form a part of a W nucleus in the via-hole, where the fluorine compound has a reducing function and a cleaning function.

Yamaha discloses a multi-layer wiring structure of an integrated circuit, and a method of manufacturing the multi-layer wiring structure. Yamaha discloses that an insulating film 12 is formed on a substrate 10, and then, a barrier layer 14 is formed on the insulating film 12. An Al layer 16 is then formed on the barrier layer 14, and an antireflection layer 18 is formed on the Al layer 16 (see paragraphs [0065]-[0066] and [0073] and Figures 1-2). A lower wiring layer 20 is then formed from a portion of the barrier layer 14, the Al layer 16 and the antireflection layer 18, and an interlayer insulating film 22 is then formed on the lower wiring layer 20 (see paragraphs [0081]-[0082] and Figures 3-4).

Yamaha also discloses that a contact hole 22a is formed through the insulating film 22. Yamaha discloses that a tight adhesion layer 24, which consists of a Ti layer 24a, a TiN layer 24b, a TiON layer 24c and a TiN layer 24d that are formed in succession, is formed on the surfaces of the contact hole 22a and the insulating film 22 to coat these surfaces (see Figure 6). A W nucleus, which is formed by SiH_4 and WF_6, is then formed in the contact hole 22a. Yamaha discloses that the tight adhesion layer 24 prevents the WF_6 from permeating into the Al layer 16 while the W plug 22a is formed (see paragraphs [0030]-[0031], [0035], [0098], [0100] and Figures 7-9).

Accordingly, Yamaha clearly does not even contemplate the problem addressed by the present invention of removing undesired materials (TiOx) from the contact hole 22a. Furthermore, the Applicants respectfully submit that the Examiner is incorrectly relying on paragraphs [0101]-[0105] of Yamaha to find an anticipating disclosure of feeding a single fluorine compound gas having a "reducing function" to clean the via-hole of undesired substances prior to the formation of the W nucleus in the via-hole. Paragraphs [0101]-[0105] of Yamaha clearly pertain to the formation of the W layer 26, and thus, clearly do not correspond to feeding a single fluorine compound gas having a "reducing function" to clean the via-hole of undesired substances (TiOx) prior to the formation of the W nucleus or the W layer.

Therefore, Yamaha clearly does not disclose or suggest feeding a single fluorine compound gas having a reducing function into the via-hole, as recited in claim 1, or feeding a single fluorine compound gas into the via-hole to clean the via-hole and to form a part of a W nucleus in the via-hole, where the fluorine compound has a reducing function and a cleaning function, as recited in claims 6 and 8.

Accordingly, Yamaha clearly does not disclose each and every limitation of claim 1, and therefore, claim 1 is clearly not anticipated by Yamaha.

As acknowledged by the Examiner, Yamaha does not even contemplate feeding a single fluorine compound gas into the via-hole to clean the via-hole prior to the formation of the W nucleus in the via-hole.

To teach this feature, the Examiner applied Nishitani et al., which discloses a removing treatment of cleaning the bottom of the via hole to remove the surface of the surface oxide layer (treatments 1-(1), 2-(1) or 3-(1)), and, an anti-corrosive treatment of

removing the corrosive cleaning substances which were produced by the removing treatment (treatments 1-(2), 2-(2) or 3-(2)). Nishitani et al. also discloses that after the removing treatment and the anti-corrosive treatment are completed, a treatment of filling small via holes with metal by means of CVD of tungsten using WF_6 and a reducing gas is performed (Column 4, line 40 to Column 5, line 10).

However, in contrast to the present invention, the removing treatment and the anti-corrosive treatment of Nishitani et al. are simultaneously performed, but with separate gases for each treatment. That is, in the removing treatment, a sputter-etching treatment with an inert gas Ar is performed, and in the anti-corrosive treatment, the insulating film surface is modified by plasma treatment using halogen-containing chemical etching gases such as Cl_2, BCl_3, CCl_4, C_2Cl_4, $SiCl_4$, NF_3, SF_6 and SiF_4 each alone or as a mixture with inert gases such as Ar (see Column 5, lines 11-19). Nishitani et al. also discloses that the anti-corrosive treatments 1-(2) and 2-(2) are accomplished by using a one-stage CVD which comprises a gas mixture of WF_6 and a reducing gas such as H_2, SiH_4 (Column 6, lines 6-17).

Accordingly, the "cleaning" operation of the via-hole of Nishitani et al. which is performed prior to the formation of the W nucleus in the via-hole consists of at least the removing treatment and the anti-corrosive treatment. As described above, the removing treatment and the anti-corrosive treatment, while performed at the same time, each use a different gas. Therefore, Nishitani et al. does not cure the deficiencies of Yamaha for failing to disclose or suggest feeding a single fluorine compound gas having a reducing function into the via-hole prior to forming the W nucleus in the via-hole, as recited in claim 1.

Furthermore, as described above, the formation of the W nucleus in the via-hole of Nishitani et al. is performed after the removing treatment and the anti-corrosive treatment are completed. Accordingly, since the formation of the W nucleus in the via-hole is performed by WF_6 gas and a reducing gas, and since the removing treatment and the anti-corrosive treatment individually use different gases, Nishitani et al. clearly does not disclose or suggest feeding a single fluorine compound gas into the via-hole to clean the via-hole and to form a part of a W nucleus in the via-hole, where the fluorine compound has a reducing function and a cleaning function, as recited in claims 6 and 8.

Therefore, Nishitani et al. clearly does not cure the deficiencies of Yamaha for failing to disclose or suggest each and every limitation of claims 6 and 8.

Accordingly, neither Yamaha nor Nishitani et al. disclose or suggest, either individually or in combination, each and every combination of claims 1, 6 and 8. Thus, no obvious combination of Yamaha and Nishitani et al. would result in the inventions of claims 1, 6 and 8 since Yamaha and Nishitani et al. clearly do not disclose or suggest, either individually or in combination, each and every limitation of claims 1, 6 and 8.

Therefore, claims 1, 6 and 8 are clearly patentable over Yamaha and Nishitani et al.

Furthermore, despite the Examiner's assertion to the contrary, the Applicants respectfully submit that it would not have been obvious to combine or modify Yamaha and Nishitani et al. to result in the inventions of claims 1, 6 and 8. Notwithstanding the fact that Yamaha and Nishitani et al. do not disclose or suggest each and every limitation of claims 1, 6 and 8, the references must suggest each and every limitation of the claims for *prima facie* obviousness under 35 U.S.C. § 103(a). The Examiner is respectfully reminded that an obviousness rejection cannot be based on the resort of the Examiner to various non-pertinent references and the combination of *bits and pieces of the references* in light of the Applicants' teachings.

Yamaha discloses a method which uses a tight adhesion layer consisting of sequentially laminated layers of Ti, TiN, TiON and TiN layer for preventing the diffusion of WF_6 while W is deposited to produce the W plug so as to reduce resistance between layers. Nishitani et al., however, is directed to a markedly different technology of filling via holes on an insulating film on a wafer to expose parts of the underlayer of the wafer by means of CVD.

Accordingly, the Applicants respectfully submit that it is improper for the Examiner to assert that it would have been obvious to modify bits and pieces of these non-related and non-pertinent references to arrive at, or otherwise render obvious, the inventions of claims 1, 6 and 8. Moreover, as clearly set forth in *Aqua-Aerobic Systems, Inc. v. Richards of Rockford, Inc.*, 1 U.S.P.Q.2d 1945, 1955-57 (N.D. Ill. 1986 (citing *In re Gordon*, 733 F.2d 900, 902, 221 U.S.P.Q. 1125 (Fed Cir. 1984), the fact that prior art references can be modified to show a claimed invention does not make the modification

obvious unless the prior art references *suggest the desirability* of the modification. The Applicants submit that no suggestion to modify or combine the teachings of Yamaha and Nishitani et al. were found in either of these references.

Therefore, it is submitted that the claims 1, 6 and 8, as well as claims 2-5, 7 and 9-20 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

A fee and a Petition for a three-month Extension of Time are filed herewith pursuant to 37 CFR § 1.136(a).

Respectfully submitted,

Hiromi OGASAWARA et al.

By: Jonathan R. Bowser

Jonathan R. Bowser
Registration No. 54,574
Attorney for Applicants

JRB/ck
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
February 11, 2005

Version with Marking
Show Changes Made

METHOD OF MANUFACTURING A SEMICONDUCTOR ELEMENT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a method of manufacturing semiconductor elements, and more particularly to a method of fabricating semiconductor elements having a multi-wiring-layer structure (multi-level interconnection structure) in which~~, with~~ a metal-filled low-resistance via-hole is ~~being~~ formed in an interlayer dielectrics (insulating film).

2. Description of the Related Art

A conventional method for fabricating semiconductor elements is disclosed in, for example, Japanese Patent Kokai (Laid-open Publication) No. 11-260823.

FIG. 6 of the accompanying drawings illustrates a cross sectional view of a semiconductor element which is fabricated by such a conventional method.

In ~~this figure~~ FIG. 6, reference numeral 1 designates a Si substrate, reference numeral 2 designates an insulating film (thin layer), reference numeral 3 designates a first wiring layer, reference numeral 4 designates an interlayer dielectrics (insulating film), reference numeral 5 designates a via-hole, reference numeral 6 designates an adhesive layer, reference numeral 7 designates a W plug, and reference numeral 8 designates a second wiring layer.

As understood from FIG. 6, the insulating layer 2, the first wiring layer 3, and the interlayer dielectrics 4 are formed on the Si substrate 1 in this order. The interlayer dielectrics 4 has the via-hole 5 which is formed by a photolithographic process and an etching process. The wall of the via-hole 5 is covered with the adhesive layer 6, and the W plug 7 is formed in the via-hole 5. After the via-hole 5 is filled with the W plug 7, the second wiring layer 8 is formed.

A process for forming the W plug 7 has two major steps. One step is a W nucleus (seed) forming step and the other ~~another~~ step is a W main portion forming step (i.e., W fill-in step).

FIG. 7 of the accompanying drawings illustrates a flowchart of a process for forming the W plug with supplied gases.

The first step is a nucleation step for forming a W nucleus for the W plug 7 (sub-steps S1 and S2). In this step, layers are formed by using WF_6, SiH_4, and H_2, which are the main raw materials.

Specifically, in the first step, a wafer (Si substrate) is placed in a chamber (a device for forming the W plug) and is then heated to a temperature which is suitable for the W plug formation. Subsequently, a raw material gas SiH_4 is fed to the chamber to form a Si layer on an adhesive layer, and then another raw material gas WF_6 is additionally fed to the chamber

to form a thin W film on the Si layer. This thin W film is called a W nucleus or seed. The WF_6 gas and the SiH_4 gas form the thin W film on the Si layer. It should be noted that the combination of the Si layer and the thin W film may be referred to as a "W nucleus."

The second step is a step for forming a main W portion (sub-step S3). In this step, the supply of the SiH_4 gas is stopped, and the W plug 7 is formed by using WF_6 and H_2 as the main raw materials.

In this procedure, after W films are formed in and over the via-hole 5 by a CVD (chemical vapor deposition) process, the surface is etched back to have only the W plug 7 remain ~~remained~~ in the via-hole 5.

When the via-hole 5 is provided on the first wiring layer 3, undesired substances 9, such as TiOx, which result in high resistance, often remain on the first wiring layer 3. If these substances 9 remain in the via-hole 5 (or between the adhesive layer 6 and the W plug 7), the resulting semiconductor element (or the via-hole) has a high resistance.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method for manufacturing a semiconductor element which ~~that~~ can eliminate high resistance substances from a via-hole so that the semiconductor element has a low resistance and high reliability.

According to a first aspect of the present invention, there is provided an improved method for manufacturing a semiconductor element. The semiconductor element has a lower wiring layer and an upper wiring layer. The lower and upper wiring layers communicate with each other by a via-hole. A fluorine compound gas having a reducing function is supplied into the via-hole to clean the via-hole. ~~After that~~ Then, a W nuclei is formed in the via-hole, and a W main portion is formed in the via-hole by, for example, a CVD process.

The fluorine compound gas has a cleaning function. The fluorine compound gas includes, for example, a WF_6 gas, a NF_3 gas, or a SiF_4 gas.

According to a second aspect of the present invention, there is provided another improved method for manufacturing a semiconductor element. The semiconductor element has a lower wiring layer and an upper wiring layer. These layers communicate with each other by a via-hole. After the via-hole is formed, a fluorine compound gas having a reducing function and a cleaning function is supplied into the via-hole to clean the inside of the via-hole and to form a part of a W nucleus in the via-hole. Subsequently, the remainder of the W nucleus is formed. After the W nucleus is formed, a W main portion is formed in the via-hole by, for example, a CVD process. The fluorine compound gas includes, for example, a SiF_4 gas.

According to a third aspect of the present invention,

there is provided still another improved method for manufacturing a semiconductor element. The semiconductor element has a lower wiring layer and an upper wiring layer. These layers communicate with each other by a via-hole. After the via-hole is formed, a fluorine compound gas having a reducing function and a cleaning function is supplied into the via-hole to clean the inside of the via-hole and to form a part of a W nucleus. Subsequently, suitable gases, such as a SiH_4 gas and WF_6 gas, are supplied into the via-hole to form the remainder of the W nucleus. A W main portion is then formed by, for example, a CVD process.

Since unnecessary substances are removed from the via-hole before the W nucleus is formed, the via-hole and the semiconductor element can have a low resistance and high reliability.

Other objects, aspects and advantages of the present invention will become more apparent to those skilled in the art from the following detailed description and the appended claims when, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross sectional view of a semiconductor element which is fabricated according to an embodiment of the present invention;

FIG. 2 is a flowchart showing a process for forming a W plug in a via-hole of the semiconductor element shown in FIG. 1

according to a first embodiment of the present invention;

FIG. 3 is a flowchart showing a process for forming the W plug in the via-hole according to a second embodiment of the present invention;

FIG. 4 illustrates a flowchart of a process for forming the W plug in the via-hole according to a third embodiment of the present invention;

FIG. 5 illustrates a flowchart of a process for forming the W plug in the via-hole according to a fourth embodiment of the present invention;

FIG. 6 is a cross sectional view of a conventional semiconductor element which is fabricated by a conventional method; and

FIG. 7 illustrates a flowchart of a process for forming a W plug in a via-hole of the semiconductor element shown in FIG. 6.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will now be described in detail.

First Embodiment

A first embodiment of the present invention is described with reference to FIG. 1 and FIG. 2. FIG. 1 shows a cross sectional view of a semiconductor element of the first embodiment.

As shown in FIG. 1, an insulating layer 12, a first wiring

layer 13, and an interlayer dielectrics (insulating film) 14 are disposed on a Si substrate 11 in that order. The interlayer dielectrics 14 has a via-hole 15 which is formed by a photolithographic process and an etching process. The wall of the via-hole 15 is covered with an adhesive layer 16, and the via-hole 15 has a W plug 17 formed therein. The W plug 17 is created by vapor deposition. Reference numeral 18 represents a second wiring layer.

The procedure of filling the via-hole 15 with the W plug 17 (i.e., the process for forming the W plug 17) will be described with reference to FIG. 2.

FIG. 2 is a flowchart of the process for forming the W plug with gases which are supplied into the via-hole 15.

After the via-hole 15 is formed, the inside (particularly the bottom) of the via-hole 15 is cleaned by a sputtering process using, for example, Ar gas. The adhesive layer 16 is then formed over the wall of the via-hole 15. Subsequently, the inside (particularly the bottom) of the via-hole 15 is further cleaned by a pre-treatment (additional cleaning step). After the pre-treatment, the W plug 17 is formed by a CVD process to fill the via-hole 15.

In the first embodiment of the present invention, as shown in FIG. 2, the WF_6 gas is used to perform the pre-treatment cleaning step (sub-step S11) prior to the nucleation step (sub-steps S12 and S13). Subsequent to the pre-treatment (sub-step

S11), the nucleation step (sub-steps S12 and S13) is conducted by using SiH_4 and WF_6, and the W deposition step (Step S14) is then conducted by using H_2 and WF_6 in the same manner as the conventional method.

Specifically, a wafer (Si substrate) is placed in a chamber (a device for forming the W plug) and is then heated to a temperature which is suitable for the W plug formation. Subsequently, the gas SiH_4 is fed to the chamber to form a Si layer on the adhesive layer 16, and then another raw material gas WF_6 is additionally fed to the chamber to form the thin W film on the Si layer 11. Subsequently~~After that~~, the gas SiH_4 is stopped, and the WF_6 gas and the H_2 gas are supplied to the chamber to deposit the W.

Since the sub-step S11 is employed, the first embodiment has the following advantages, when compared with the conventional method.

As shown in FIG. 6, the substances 9 including TiOx, which result in high resistance, exist at the bottom of the via-hole 5 after the via-hole 5 is created in the conventional method. It is assumed that the substances 9 are formed on the first wiring layer 3 during the process of making the via-hole 5. In the first embodiment of the present invention (FIG. 2), the Ar gas is supplied into the via-hole 15 ~~5~~ to remove the substances 9 (sputtering process). However, the removal of the substances 9 by the Ar gas is often insufficient. Therefore, the WF_6 gas

is introduced into the via-hole 15 in the first step (sub-step S11) before formation of the W plug 17. The substances 9 are therefore completely removed from the via-hole 15 by a cleaning effect of the WF_6 gas having a strong reducing function. Since the substances 9 do not exist inside the via-hole 15 (FIG. 1), the product (semiconductor element) has a low resistance.

Second Embodiment

A ~~Next, a~~ second embodiment of the present invention will now be described with reference to FIG. 1 and FIG. 3.

A semiconductor element which is fabricated in accordance with the second embodiment is the same as the semiconductor element shown in FIG. 1. Thus, the structure of the semiconductor element will not be redundantly described here. The second embodiment is different from the first embodiment with respect to the process for forming the W plug 17 in the via-hole 15. Therefore, the following description principally deals with the process for forming the W plug 17.

FIG. 3 is a flowchart showing the process for forming the W plug 17 with the gases which are supplied into the ~~a~~ via-hole 15.

After the via-hole 15 is formed, the interior (particularly the bottom) of the via-hole 15 is cleaned by a sputtering process using, for example, Ar gas, and an adhesive layer 16 is then formed over the wall of the via-hole 15. Subsequently, the interior (particularly the bottom) of the

via-hole 15 is further cleaned by a pre-treatment step. A W portion 17 is then formed by a CVD process to fill the via-hole 15. The pre-treatment step is performed by using a NF_3 gas in the second ~~this~~ embodiment. The NF_3 gas has a strong reducing and cleaning function.

As mentioned above, the NF_3 gas is fed to a W forming chamber (sub-step 21) prior to the CVD process. This pre-treatment cleaning step completely removes the substances 9 from the via-hole 15. Subsequent to the cleaning step, a nucleation step (sub-steps S22 and S23) and a W deposition step (sub-step S24) are conducted in that order in the same manner as the conventional method (FIG. 6 and FIG. 7).

Since the above-described ~~above~~ procedure is employed, the following advantages can be obtained as compared with the conventional method (FIG. 6 and FIG. 7).

According to the ~~a~~ conventional method, the substances 9 such as TiOx, which create a high resistance, remain at the bottom of the via-hole 5 after the via-hole 5 is created in the conventional method. As a result, the semiconductor element has a high resistance at the via-hole 5. According to the second embodiment, however, the Ar gas is supplied into the via-hole 15 ~~5~~ to remove the substances 9 before the adhesive layer 16 is formed, and the NF_3 gas is fed into the via-hole 15 ~~5~~ to completely clean the substances 9 (sub-step S21) before the via-hole 15 is filled with the W portion 17. Therefore,

the substances 9 do not remain in the via-hole at the time of sub-steps S22 and S23. The NF_3 gas has a cleaning effect with a strong reducing function. Thus, the product (semiconductor element) can have a low resistance.

Third Embodiment

A ~~Next, a~~ third embodiment of the present invention will now be described with reference to FIG. 1 and FIG. 4. A semiconductor element which is fabricated in accordance with the third embodiment is the same as the semiconductor element shown in FIG. 1. Thus, the structure of the semiconductor element will not be redundantly described here. The third embodiment is different from the first and second embodiments with respect to the process for forming the W plug 17 in the via-hole 15. Therefore, the following description principally deals with the process for forming the W plug 17.

FIG. 4 is a flowchart showing the process for forming the W plug 17 with the gases which are supplied into the ~~a~~ via-hole 15.

After the via-hole 15 is formed, the interior (particularly the bottom) of the via-hole 15 is cleaned by a sputtering process using, for example, Ar gas, and an adhesive layer 16 is then formed over the wall of the via-hole 15. Subsequently, the interior (particularly the bottom) of the via-hole 15 is further cleaned by a pre-treatment step. A W portion 17 is then formed by a CVD process to fill the via-hole

15. The pre-treatment step is performed by using a SiF_4 gas in the third ~~this~~ embodiment.

Before the CVD process is conducted, the SiF_4 gas is fed to the chamber in the first step (sub-step 31). Subsequently, a nucleation step (sub-steps S32 and S33) and a W deposition step (sub-step S34) are conducted in that order in the same manner as the conventional method (FIG. 6 and FIG. 7).

Since the above-described ~~above~~ procedure is employed, the following advantages can be obtained as compared with the conventional method.

The substances 9 (FIG. 6) such as TiOx which create a high resistance remain at the bottom of the via-hole immediately after the formation of the via-hole 5 in the conventional method. The Ar gas is supplied into the via-hole 15 ~~5~~ to remove the substances 9 prior to the formation of the adhesive layer 16. However, the removal of the substances 9 by the Ar gas is often insufficient. Therefore, before the via-hole 15 is filled with the W portion 17, the SiF_4 gas is supplied into the via-hole 15 (sub-step S31) so as to completely remove the substances 9 from the via-hole 15. The SiF_4 gas has a strong reducing function. Thus, the resulting semiconductor element (FIG. 1) has a low resistance.

Fourth Embodiment

A ~~Next, a~~ fourth embodiment of the present invention will now be described with reference to FIG. 1 and FIG. 5. A

semiconductor element which is fabricated in accordance with the fourth embodiment is the same as the semiconductor element shown in FIG. 1. Thus, the structure of the semiconductor element will not be redundantly described here. The fourth embodiment is different from the foregoing embodiments with respect to the process for forming the W plug 17. Therefore, the following description principally deals with the process for forming the W plug 17.

FIG. 5 is a flowchart showing the process for forming the W plug 17 with the gases which are supplied into the ~~a~~ via-hole 15.

After the via-hole 15 is formed, the interior (particularly the bottom) of the via-hole 15 is cleaned by a sputtering process using, for example, Ar gas, and an adhesive layer 16 is formed over the wall of the via-hole 15. Subsequently, the interior (particularly the bottom) of the via-hole 15 is further cleaned by a pre-treatment step. A W portion 17 is then formed by a CVD process to fill the via-hole 15. The pre-treatment cleaning step is performed by using a SiF_4 gas in the fourth ~~this~~ embodiment.

Before the CVD process is conducted, the SiF_4 gas is fed to the chamber in the first step (sub-step 41) to conduct the pre-treatment cleaning. When the SiF_4 gas removes the unnecessary substances 9, the SiF_4 gas also creates the ~~a~~ Si layer. In other words, the pre-treatment and part of the

nucleation step (i.e., formation of the Si layer) are carried out at the same time. After the pre-treatment and the Si layer formation, the feeding of the SiF_4 gas is stopped, and the SiH_4 gas and the WF_6 gas are fed into the chamber to complete the nucleation step (sub-step S42). The CVD step for filling the via-hole 15 with W (sub-step S43) is then conducted.

Since the fourth embodiment uses the above-described ~~above~~ procedure, the following advantages can be obtained.

The substances 9 (FIG. 6) such as TiOx which create a high resistance often remain at the bottom of the via-hole after the via-hole 5 is created in the conventional method. The Ar gas is supplied into the via-hole 15 ~~5~~ to remove the substances 9 prior to the formation of the adhesive layer. However, the removal of the substances 9 by the Ar gas is often insufficient. Therefore, before the via-hole 15 is filled with the W portion, the SiF_4 gas is fed into the via-hole 15 (sub-step S41) to completely remove the substances 9 from the bottom of the via-hole ~~bottom~~. The SiF_4 gas has a strong reducing function. Thus, the resulting semiconductor element has a low resistance.

Furthermore, in the fourth embodiment, the Si layer is formed in the via-hole 15 by the SiF_4 gas while the inside of the via-hole 15 is being cleaned by the SiF_4 gas. That is, the cleaning can be performed together with part of the nucleus forming process. Subsequently, the remainder of the nucleus forming process is ~~done~~ completed, and the W deposition step is

conducted.

It should be noted that the present invention is not limited to the illustrated and described embodiments. Various modifications and changes can be made within the scope of the present invention, and such modifications are also included in the scope of the present invention.

ABSTRACT OF THE DISCLOSURE

A semiconductor element has an upper wiring layer and a lower wiring layer. The upper and lower wiring ~~These~~ layers communicate with each other via a via-hole. The via-hole is filled with W. Before W is filled in the via-hole by a CVD process to connect the lower wiring layer to the upper wiring layer, a cleaning gas is supplied into the via-hole to remove particular substances, which would otherwise result in high resistance. Subsequent to the cleaning step, the W portion is formed in the via-hole. Since the high resistance substances are removed from the via-hole before the formation of the W portion, the semiconductor element (or the via-hole) has a low resistance and high reliability.